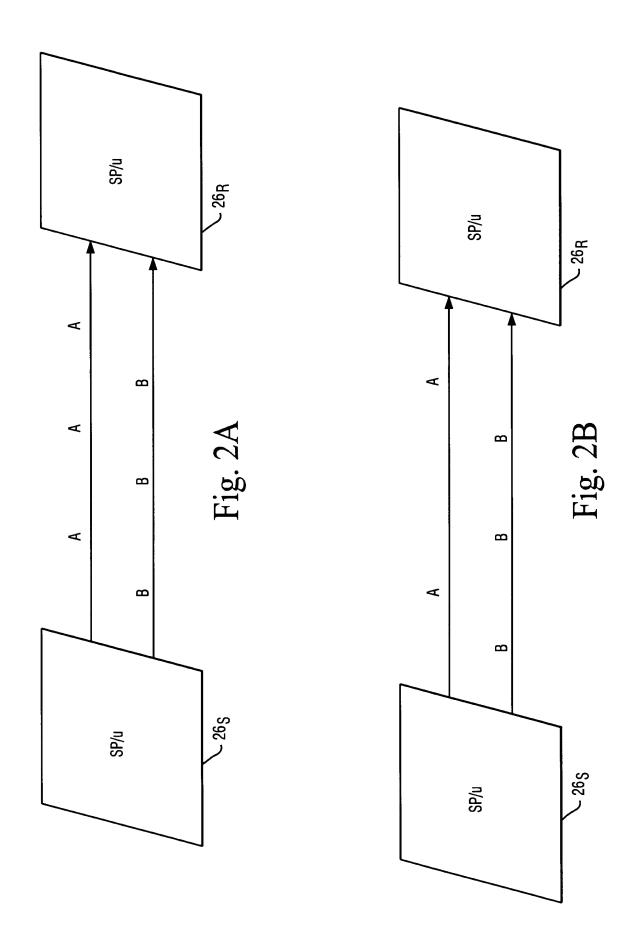
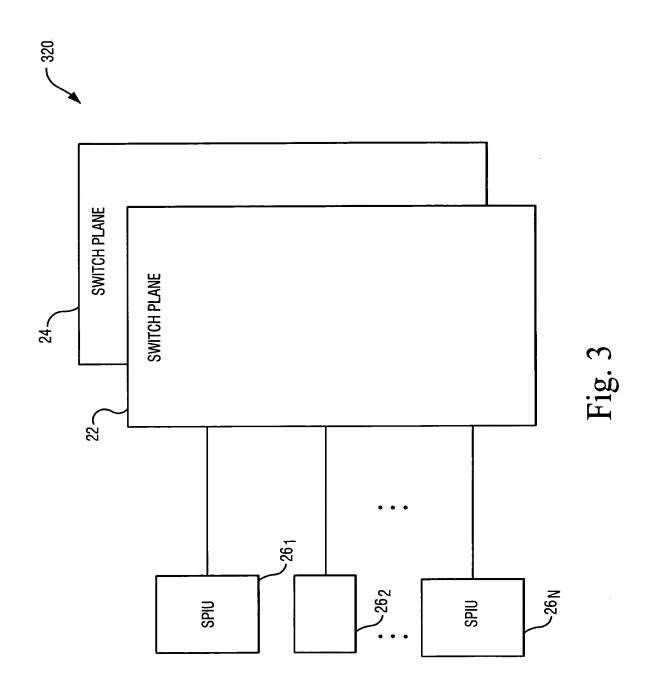
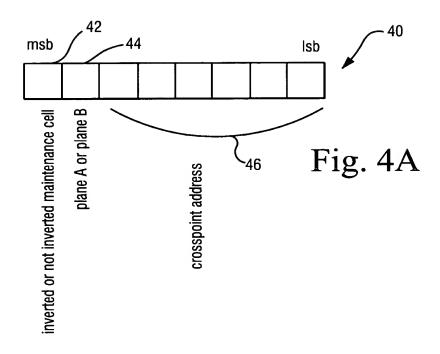
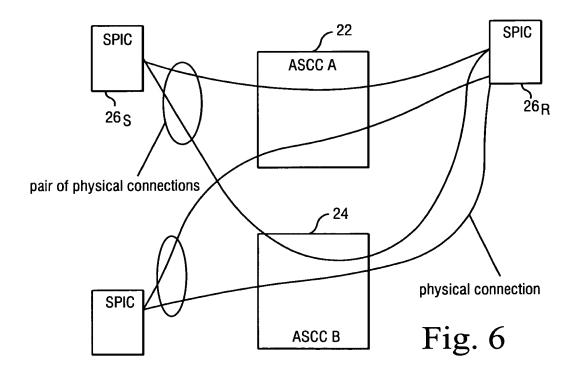


Fig. 1









		В7	B6	B5	B4	В3	B2	B1	В0			
	type QoS		S CLP		cell size			parity	4		1	
		0	0	0	0	1 .	0	1	1	1		ASCI Header
		format		doc	destination address				parity 2	2		Headel
		0	msb					Isb		_ /	/	
		format		logic address					parity	•		ı
		1	1	1	1	1	0	0	0	3		
SPAS		inv	SMC/		not defined				parity	4		
Header		0	INI	not defined				parity	4		0	
									norit.	5		
									parity	J		
									parity	6		ASCI
									ματιτή	J		Payload
									parity	7		
									parity	,		
										8		
SPAS												
		\	crosspoint test pattern								•	
Payload		ĺ										
									lsb	60		l
									130			

Fig. 4B(1) Initialisation Cell

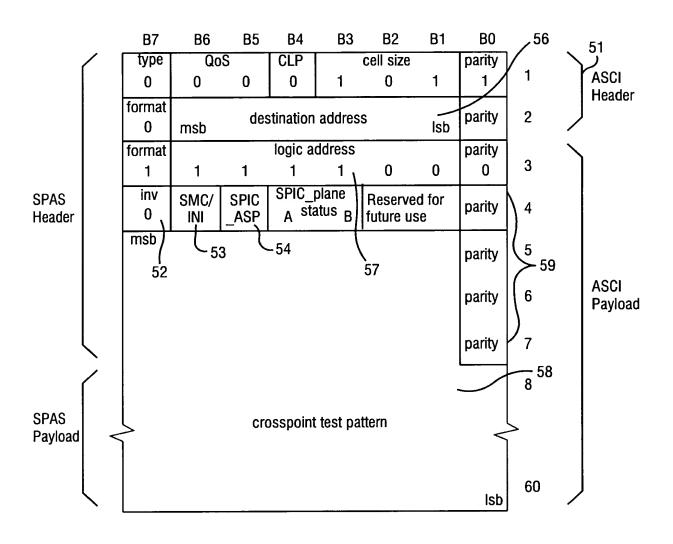
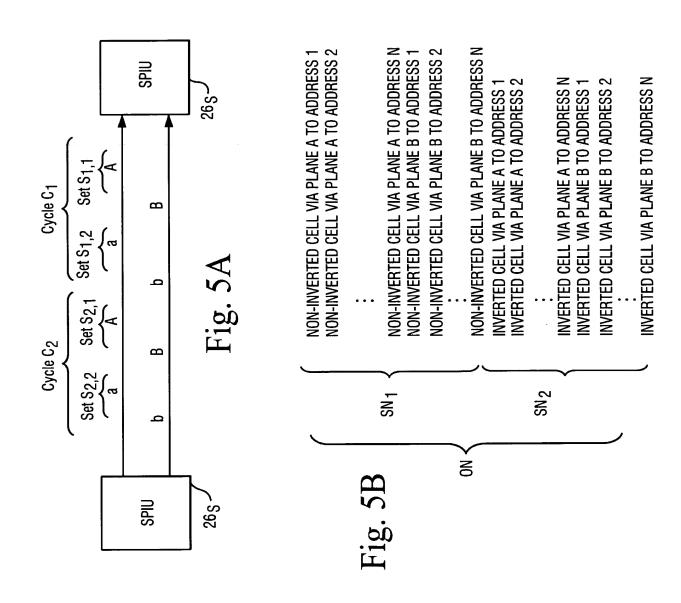
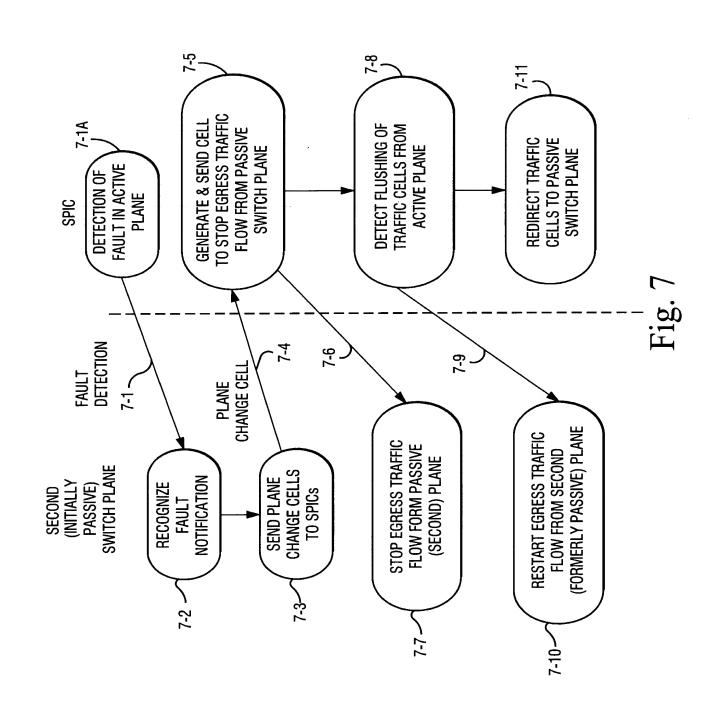
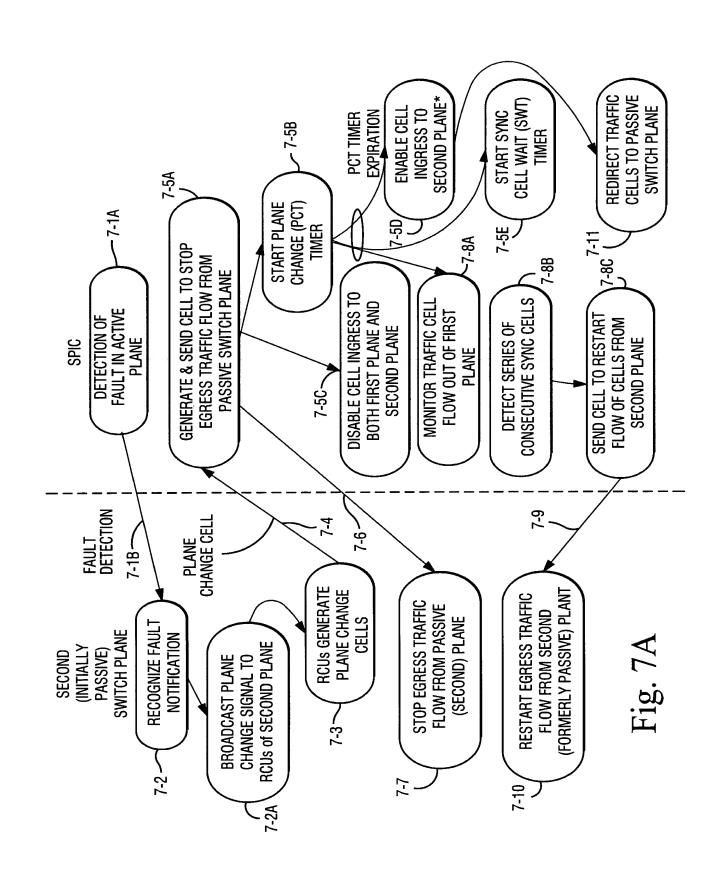
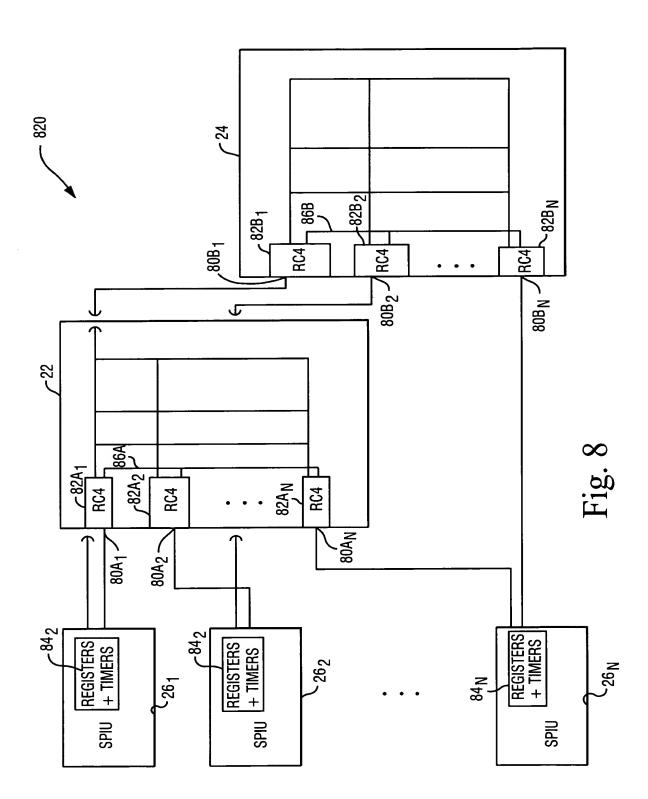


Fig. 4B(2) Initialisation Cell

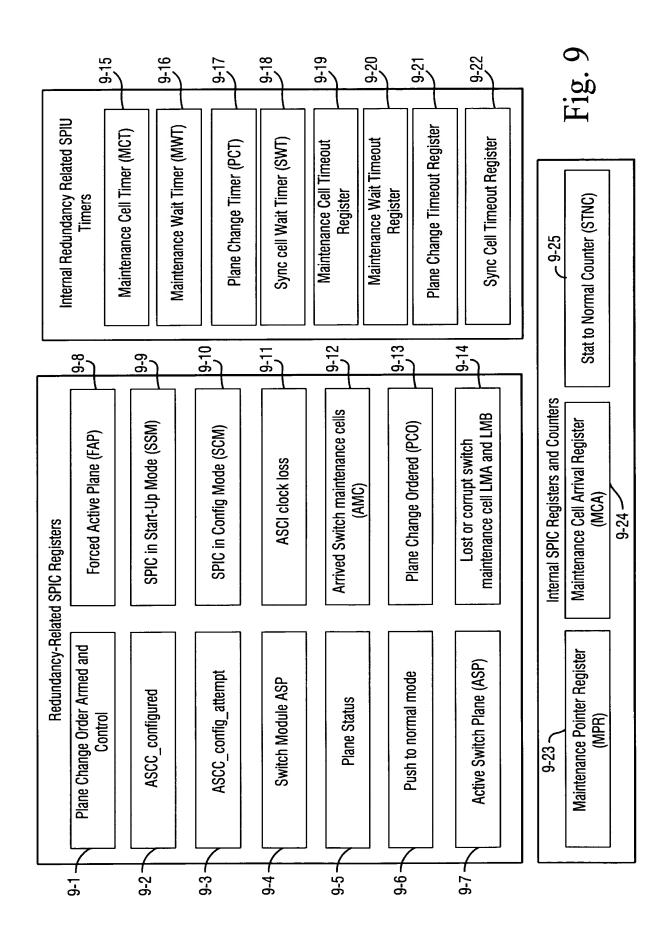








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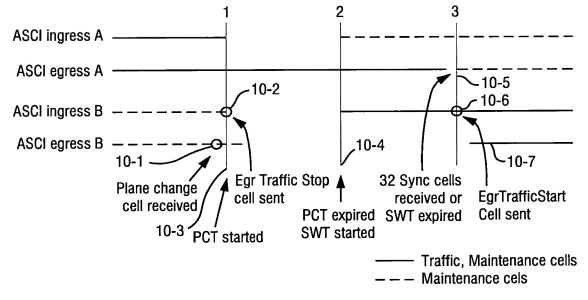
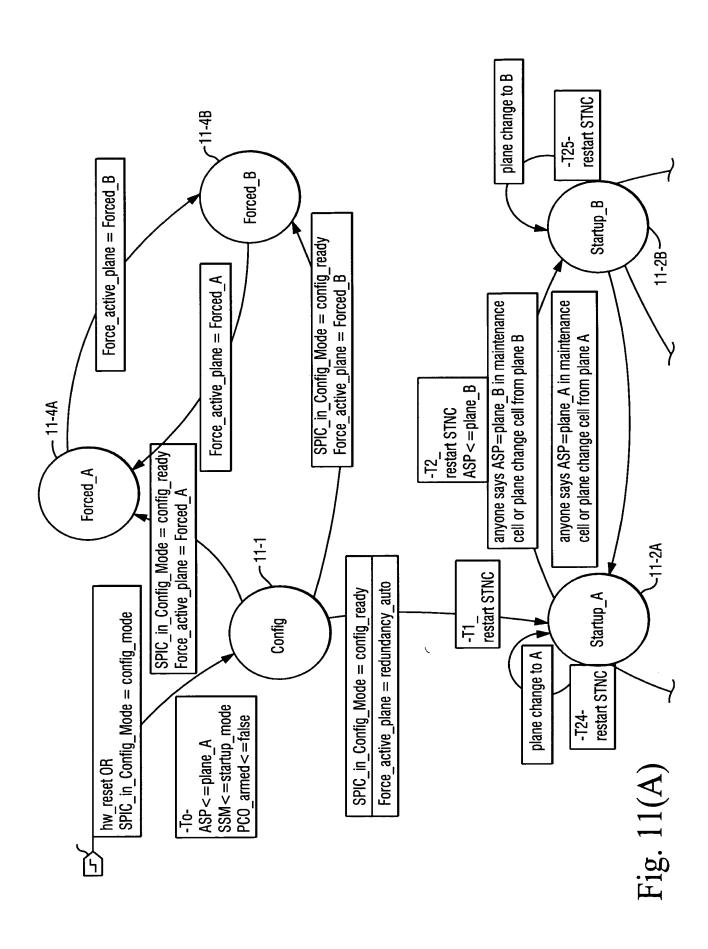
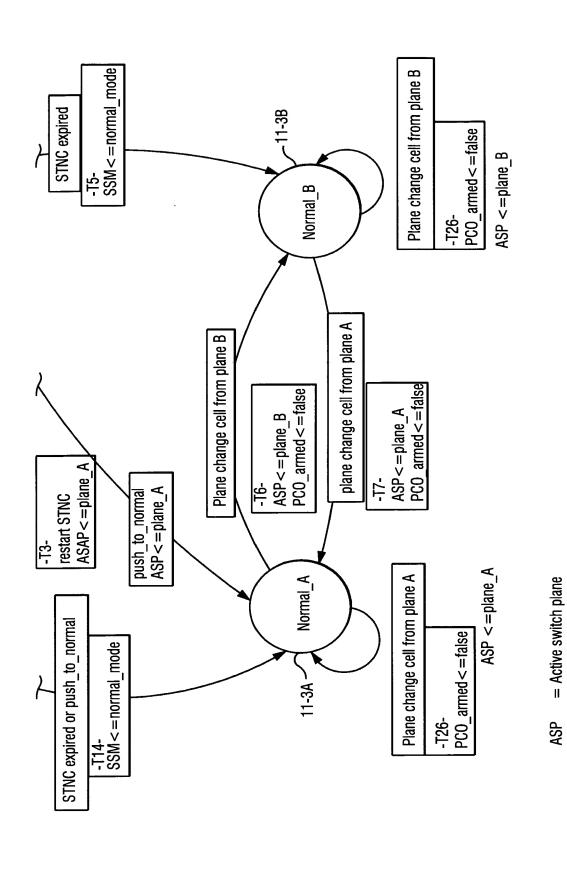


Fig. 10





 $\begin{array}{ccc} & \text{PCO} \text{ armed} = \text{Plain change order armed} \\ Fig. & 11(B) & \text{STNC} & = \text{Start to normal counter} \end{array}$

= SPIC in start-up mode

SSM

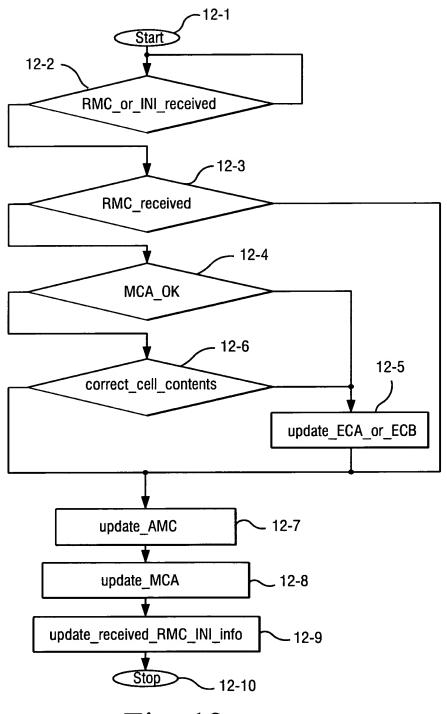


Fig. 12

